

# Vitesse Network Processors

(Sitera's PRISM IQ2000 NPU Family)

## Optimizing Architecture for Bandwidth and Flexibility

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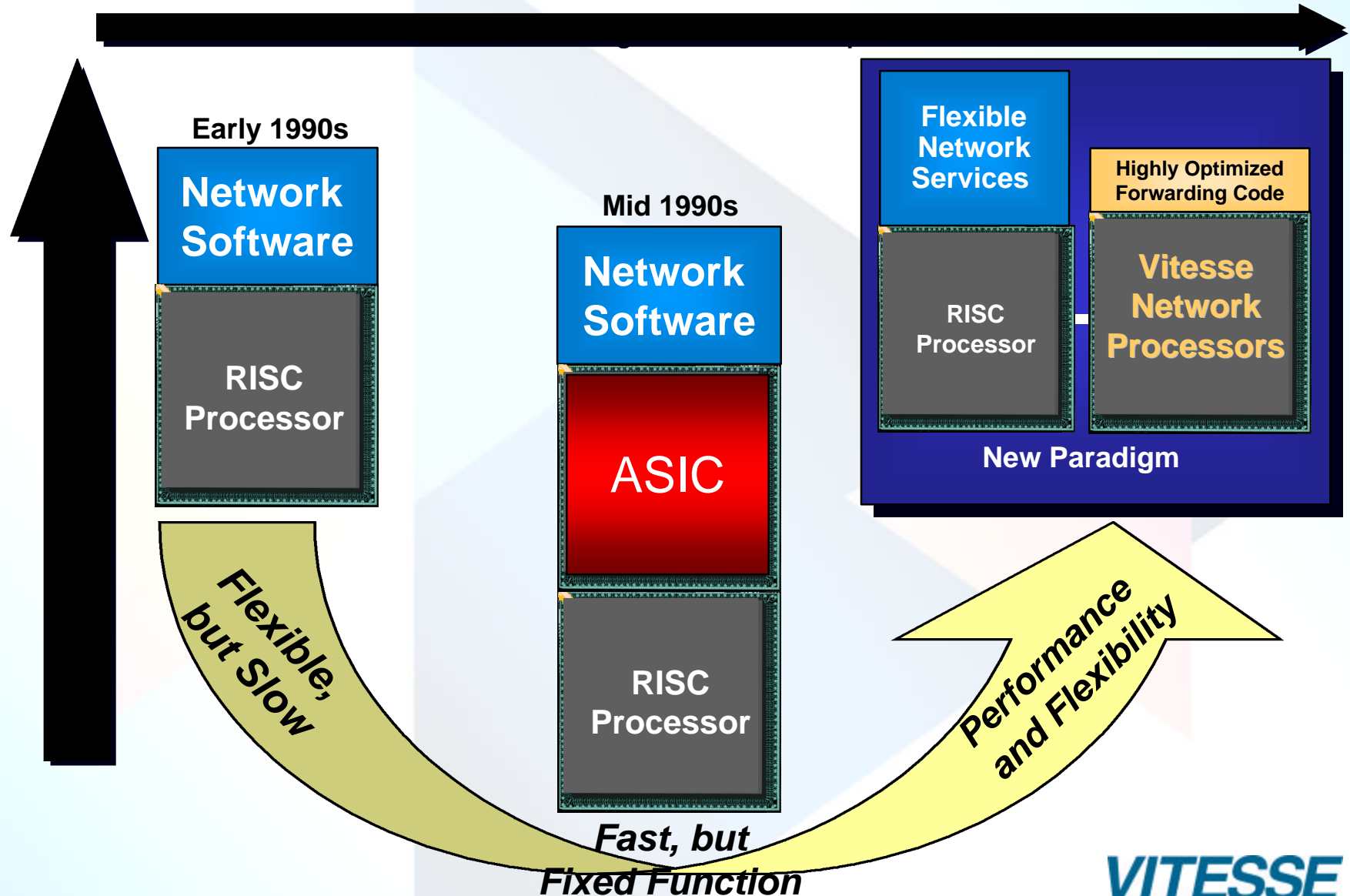
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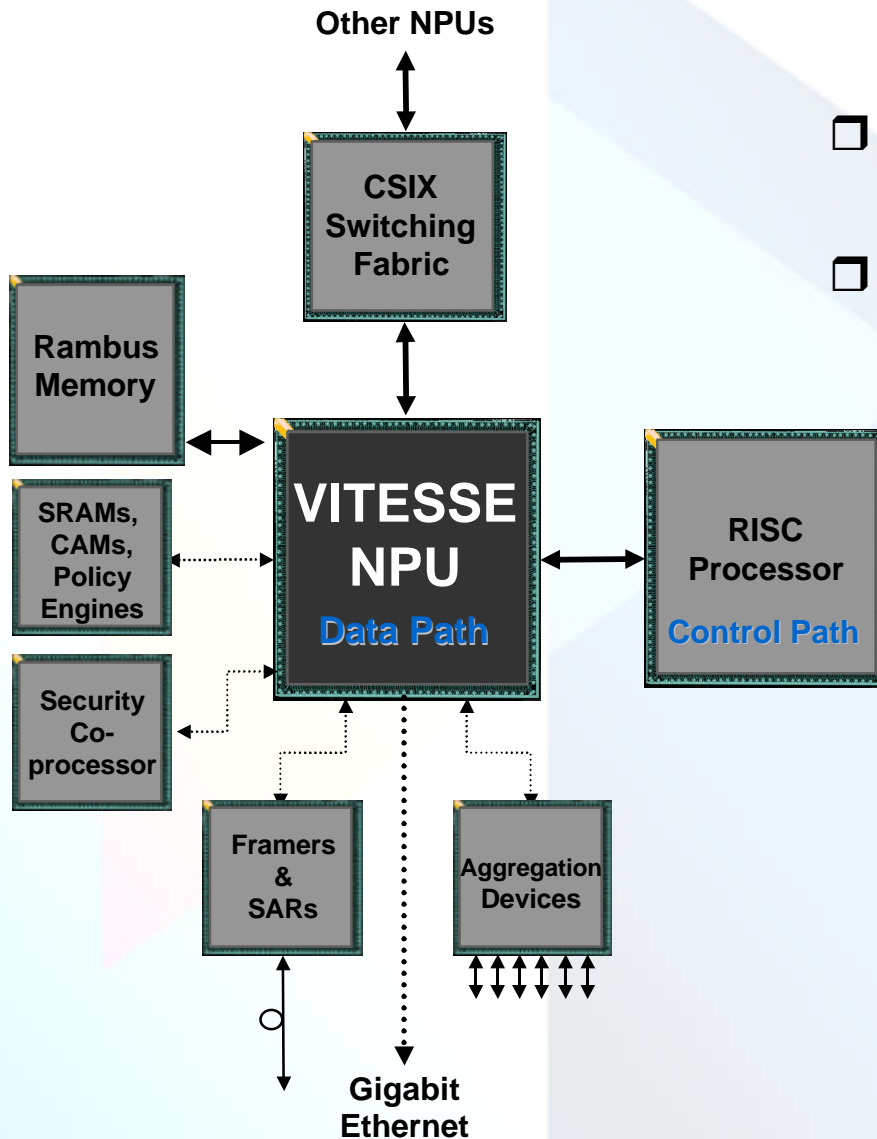
# Why Network Processors (NPUs) are Hot Chips

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# NPU-based System Solutions

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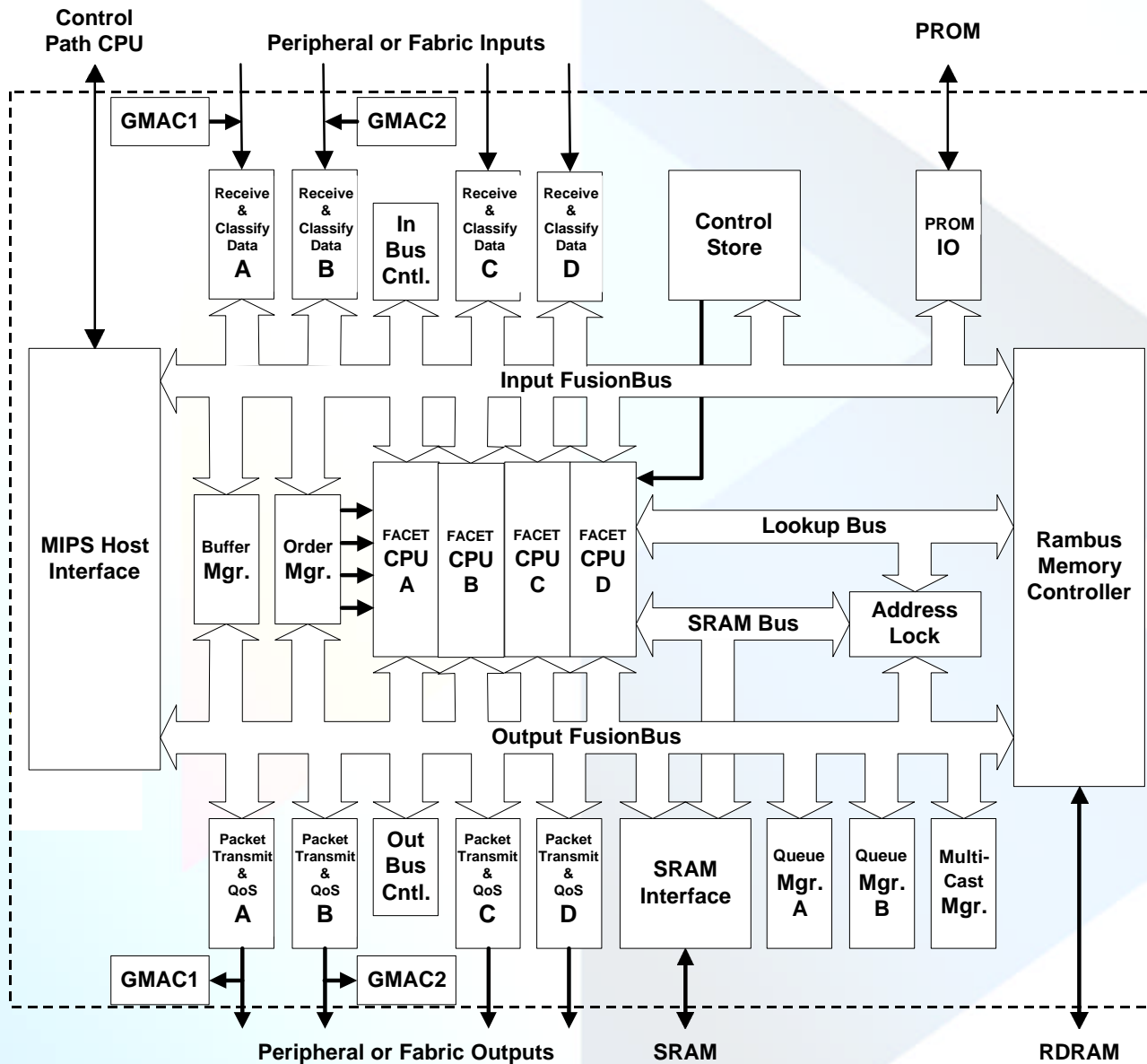
- ❑ **Data Path (Fast Path) Optimized for per Packet Operations**
- ❑ **Efficient Operations with System Components**
  - General Purpose RISC Processor for Control Path (Slow Path)
  - High Performance Memory for Data Buffering, Route Tables, etc.
  - Flexible Physical Interfacing
  - Standard Switch Fabric Interconnect
  - Special Purpose Coprocessor Interconnections

# NPU Design Objectives



- ❑ Provide the customer with the ability to differentiate their products in the market
- ❑ Flexibility for a Wide Variety of Network Applications
  - Fully Programmable
  - Simple System Connectivity
- ❑ Cost Effective
  - High Performance based on Efficient CPU utilization
  - Minimized System Components
  - Low Power Consumption

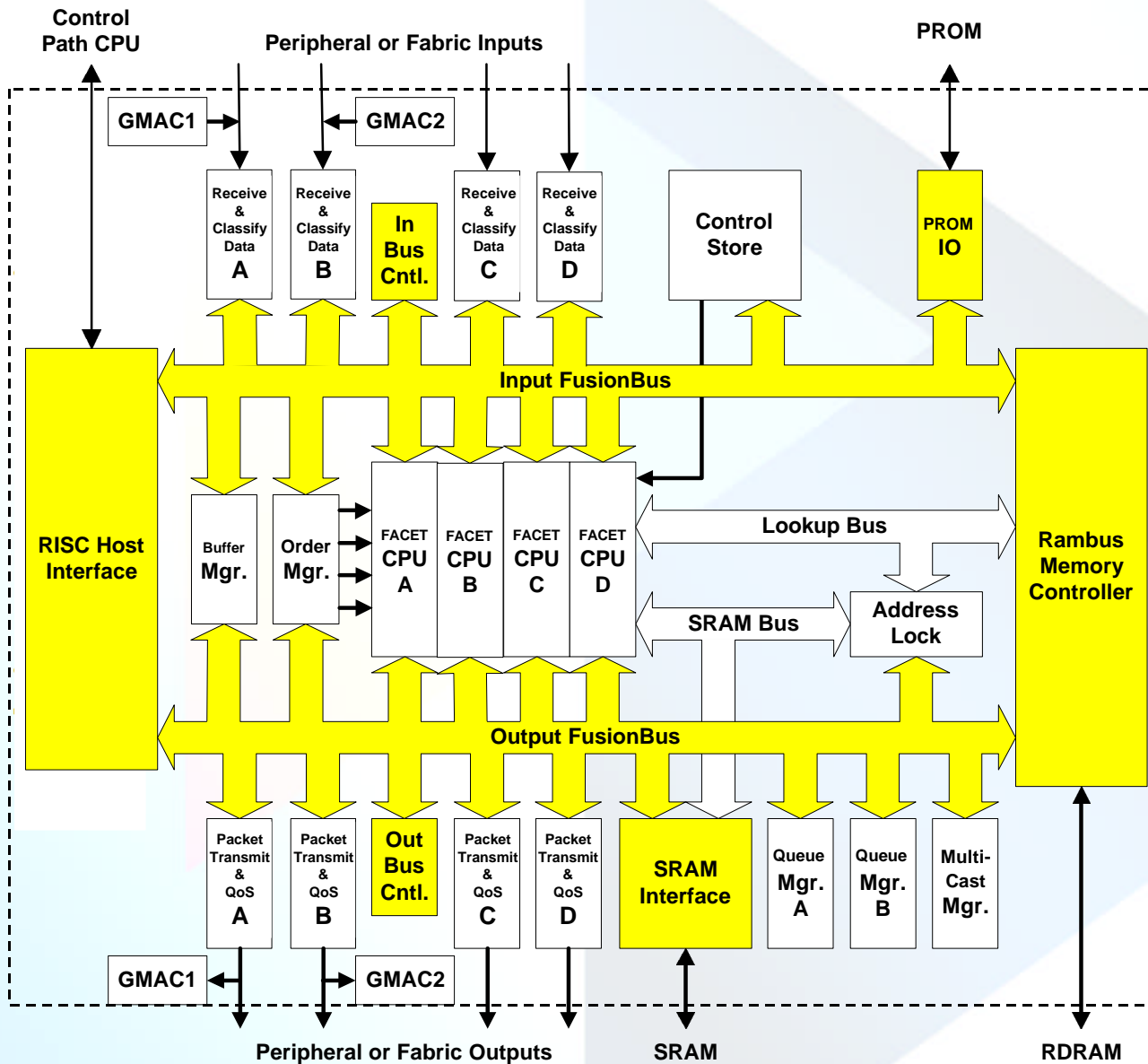
# Vitesse NPU Block Diagram



## Chip Design Focused in Three Areas

- System Functions
- Data Flow
- Packet Processing

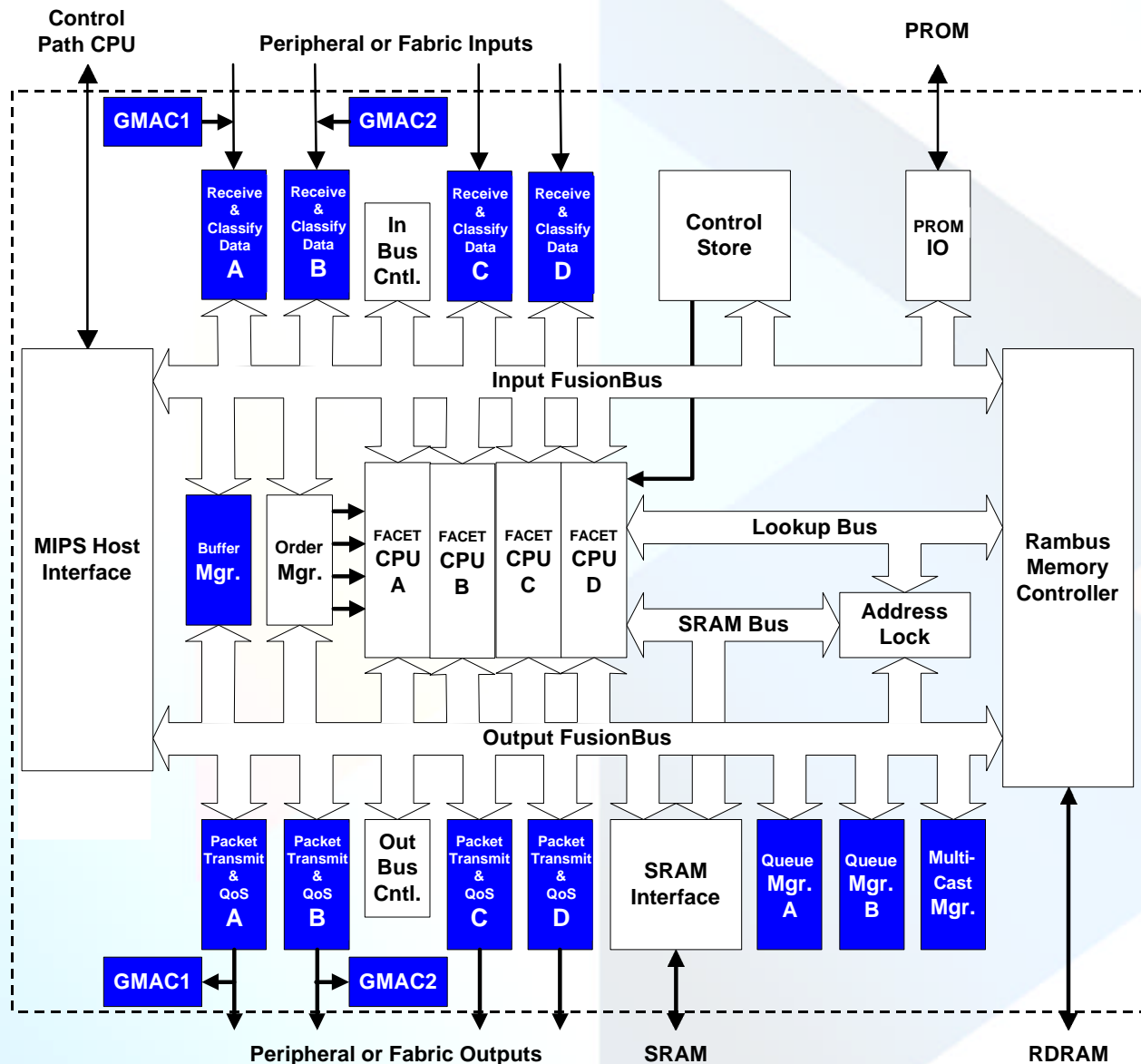
# NPU System Functions



- ❑ 25.6 Gbps Internal Bandwidth
- ❑ Modular FusionBus™ Technology
- ❑ Low Cost Rambus™ Dynamic Memory - 12.8 Gbps
- ❑ Memory Controller supports 14 outstanding memory transactions
- ❑ Flexible RISC CPU Interface
  - High Performance or Low Cost
- ❑ Optional SRAM I/F

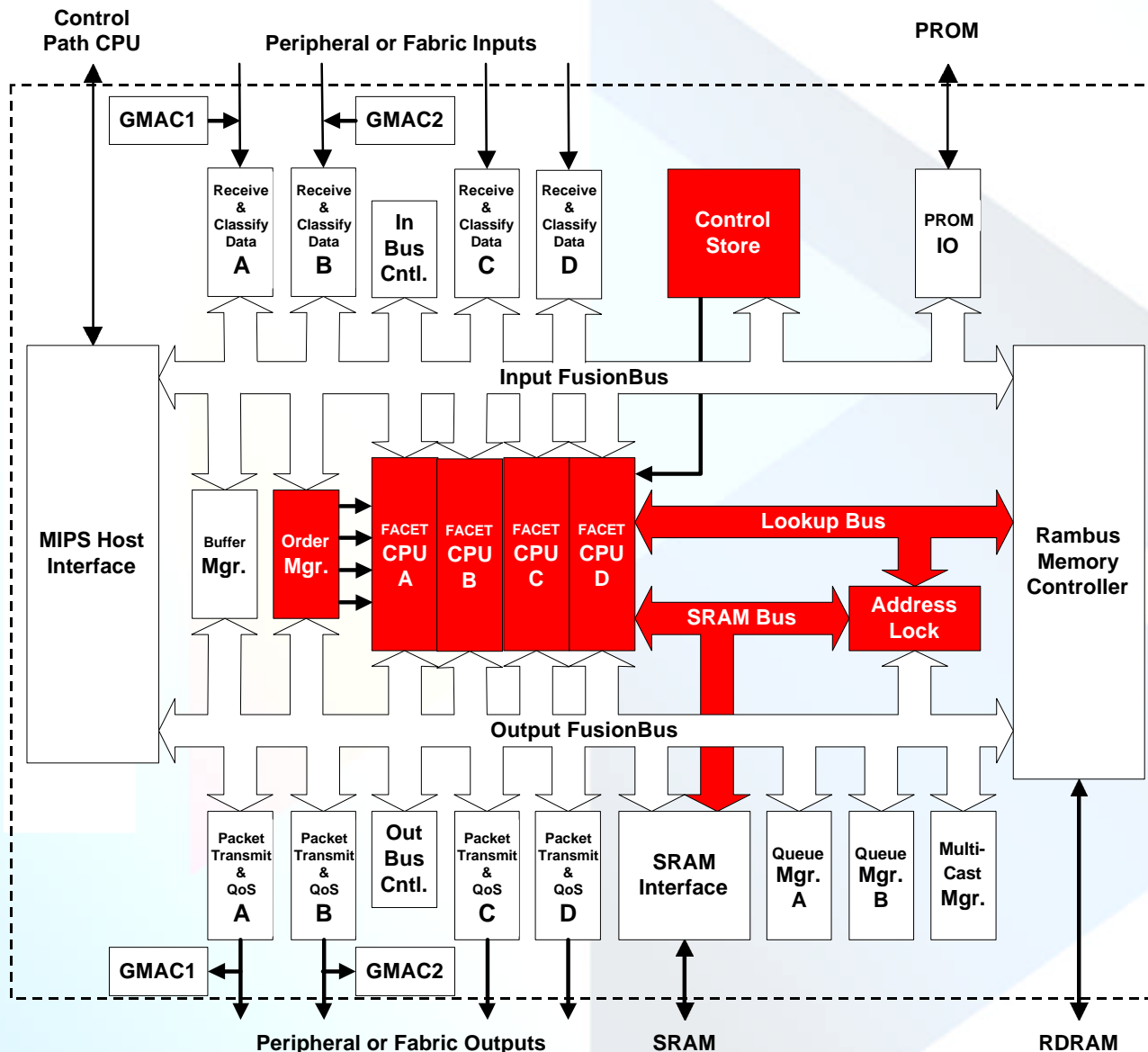


# NPU Data Flow Functions



- ❑ Off-loads Data Movement from Embedded CPUs
- ❑ Up to 12.8 Gbps Peripheral Bandwidth
- ❑ Optimized Packet Header Operations
- ❑ Packet Classification, Packet Queuing, Quality of Service (QoS) and Multicast Support
- ❑ Memory Buffer Management
- ❑ Integrated Gigabit Ethernet

# Packet Processing Functions



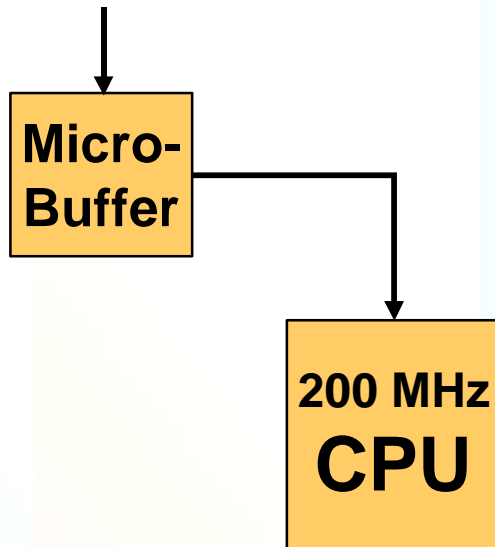
- ❑ Four 200 MHz Network Optimized Embedded RISC CPUs + Special Packet Processing Instruction Set
- ❑ Lookup, DMA, Context Manager Coprocessors
- ❑ Four User Contexts per Embedded Processor  
➡ 16 Packets Simultaneously in Process



# Networking Optimized CPU Architecture

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Control Store



- ❑ 32-bit RISC Processor
- ❑ 64-bit Memory Access
- ❑ 16 Instruction MicroBuffer
- ❑ NPU Instruction Extensions

# Network Optimized Instructions

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## ❑ **Classes of Special Instructions**

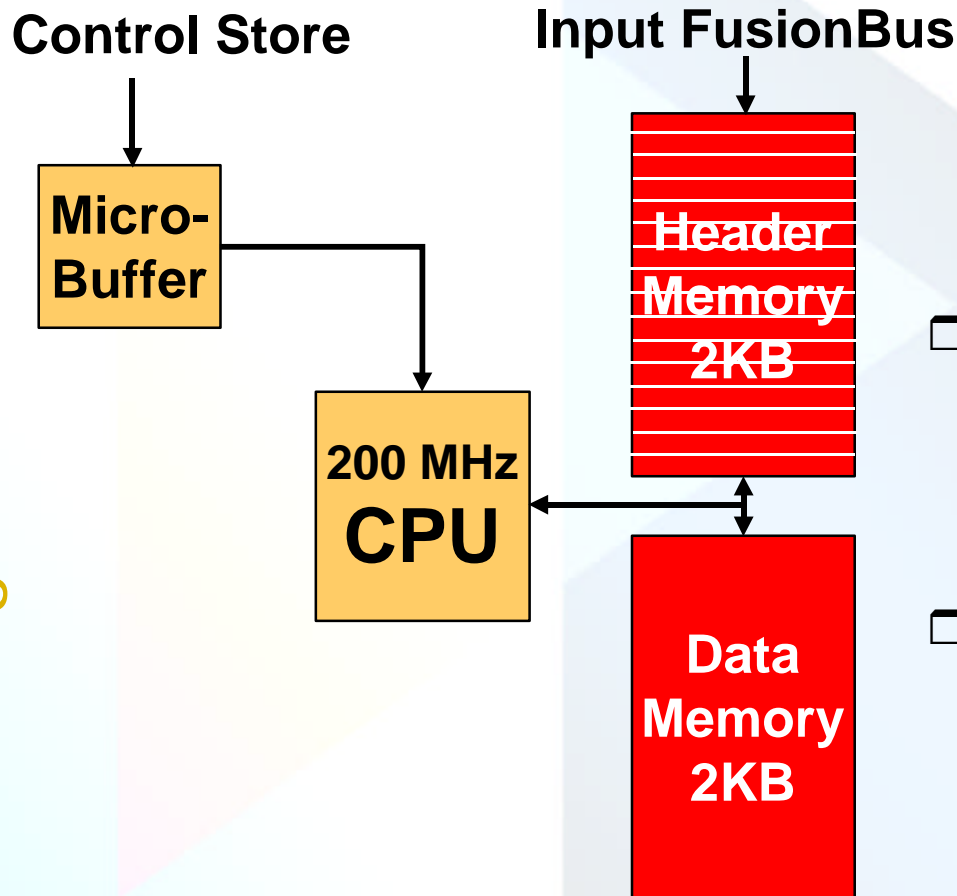
- Bit Test
- Byte Test
- Field Extract
- Enhanced Immediates
- Double Load/Store
- Special Arithmetic (16-bit 1's complement)

## ❑ **Vitesse's Implementation of an RFC 1812-compliant Router**

- 50% of the implemented instructions are NPU special instructions
- Special instructions are ~3 times as efficient as standard RISC instructions

# Networking Optimized CPU Architecture

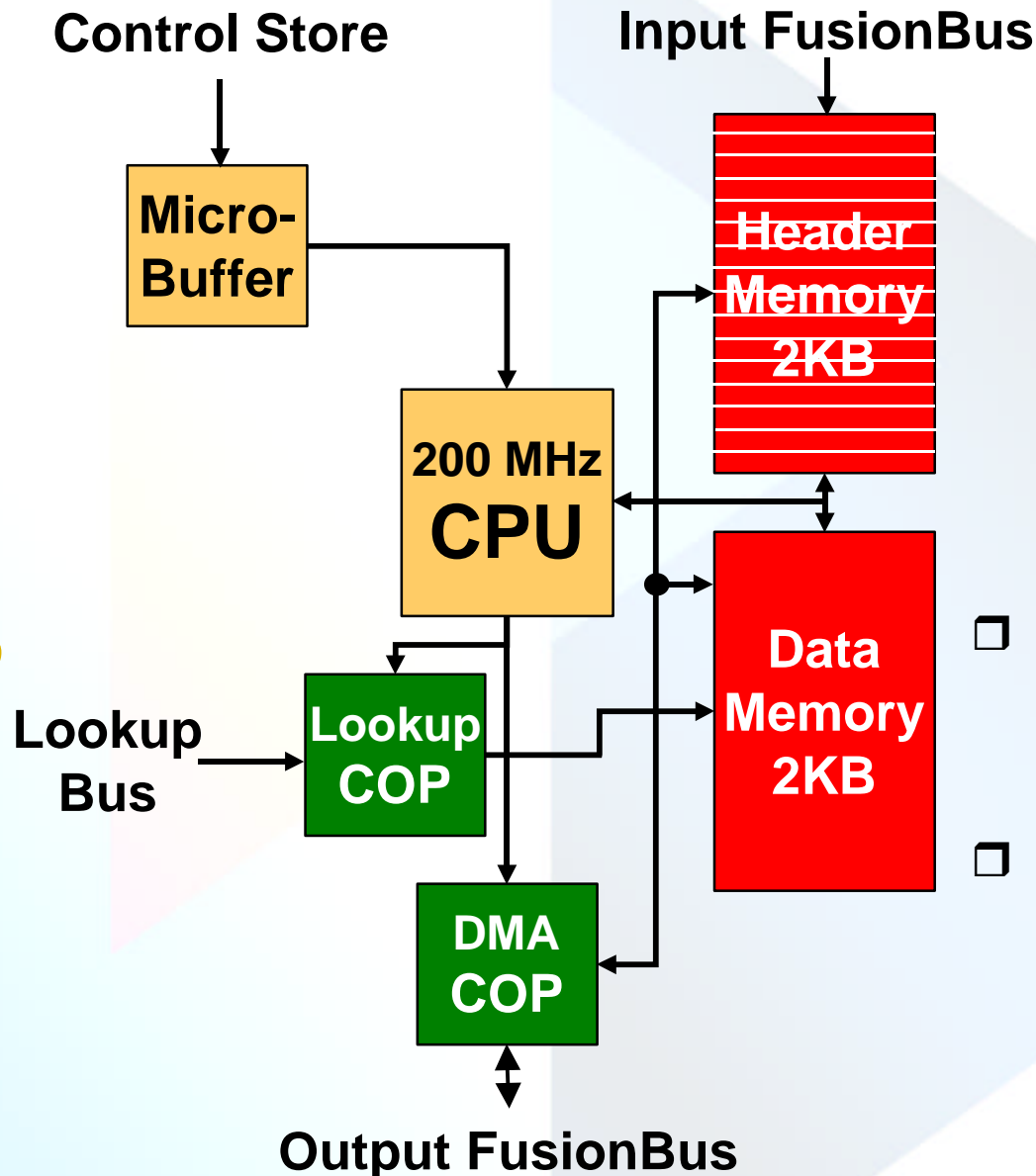
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- ❑ **2KB 64-bit Triple Ported Header Memory**
  - 16 x 128B Header Buffers
- ❑ **2KB General Purpose 64-bit, Triple Ported Data Memory**

# Networking Optimized CPU Architecture

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## ❑ Lookup Coprocessor

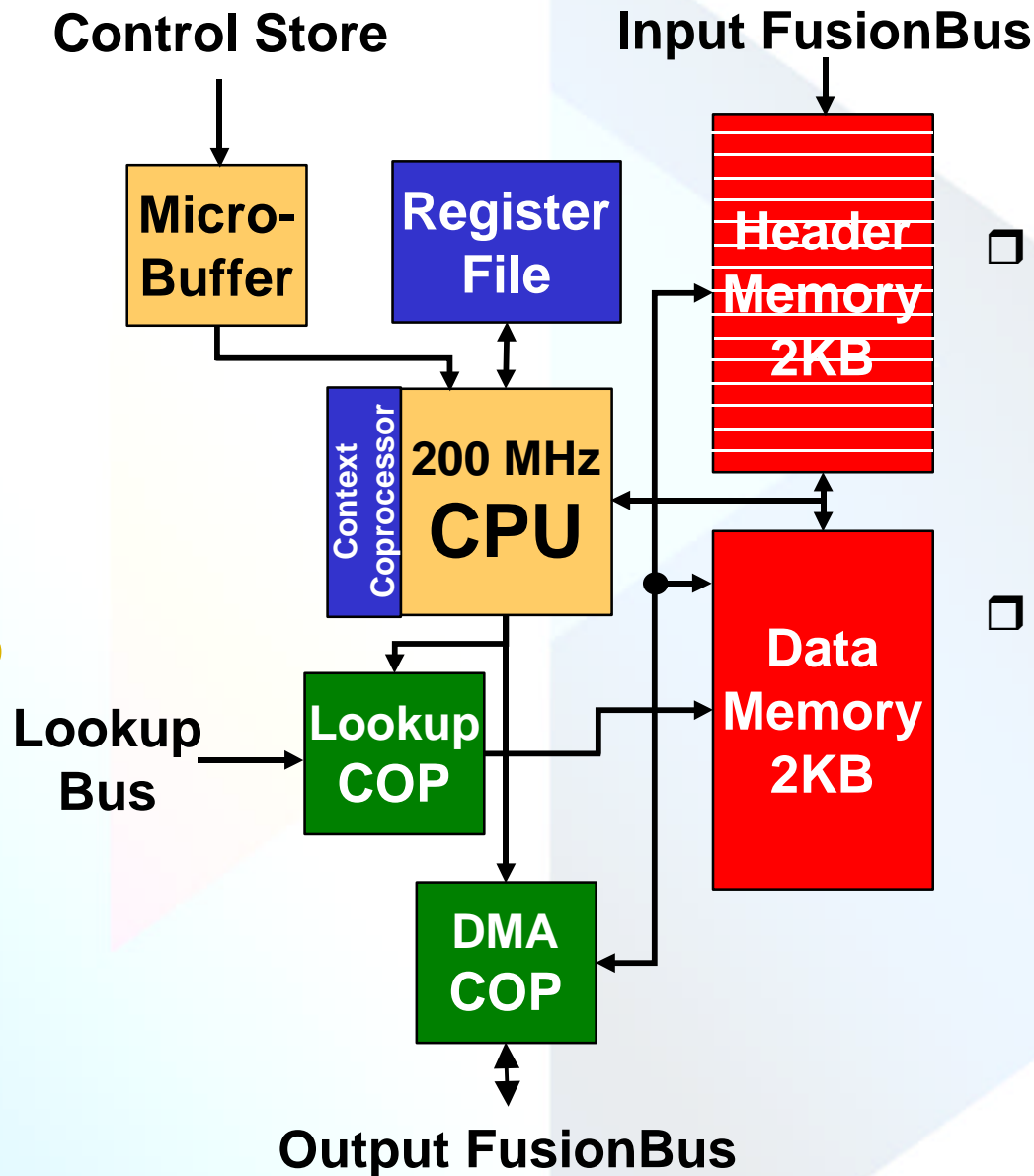
- Fixed Size, Read Only and Pipelined Direct Memory Connection
- Hash Table Acceleration

## ❑ DMA Coprocessor

- Variable size READ/WRITE Transfers
- Access to all Output FusionBus Modules, including Memory

# Networking Optimized CPU Architecture

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- ❑ **Five Context Register File**
  - 32 32-bit Registers for each context
  - Four User Contexts
  - One Kernel Context
- ❑ **Hardware Assisted Context Switching**

# Simplified Multi-processing

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- ❑ Multi-processor and Multi-Threaded Hardware for Performance Optimization
- ❑ Single Threaded Software for Ease of Programming
- ❑ Example Code

```
...  
RXR      R3,R4      //Start a DMA transfer  
                (possible context switch if DMA queue full)  
ORUI     R5, 0x0040  //Set a flag  
TRAPQNE  //Check for result available  
                (context switch on no results available)  
...
```

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# Next Generation NPUs

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- ❑ **Customers Continue to Demand the Acceleration of Bandwidth and the Flexibility, which allows them to Deliver a Wide Variety of Connectivity and Services**
- ❑ **Process Technology Advancements Enables More Transistors**
- ❑ **Vitesse's Modular Architecture for System-on-Chip Design Makes It Easy to Enhance Performance and Features**
  - More Processors for Raw Performance
  - More Peripheral Interfaces for Data Throughput
  - More Memory Bandwidth for Support of Services
  - Additional Special Purpose Coprocessors for Advanced Features